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EXAMINER	
TRINH, MICHAEL MANH	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/678,417	**Applicant(s)** FAN ET AL.
	Examiner Michael Trinh	**Art Unit** 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12,14-19 and 21* is/are pending in the application.

4a) Of the above claim(s) *12,14 and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed March 19, 2007. Claims 12,14-19,21 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Election/Restrictions

1. This application contains claims directed to the following patentably distinct species:

Newly submitted claim 21 together with claims 12,14 are drawn and directed to a first species having a subject matter that are distinct from originally claimed species in original claims 15-19 for the following reasons: a) Group I, originally claimed claims 15-19, is drawn and directed to a process of an integrated circuit package (e.g. as shown in Figure 5F) including a first claimed species of mounting a die adapter to the semiconductor device; and b) Group II, newly added claim 21 together with claims 12,14 is newly drawn and directed to a process of fabricating an integrated circuit package (e.g. as shown in Figure 6) including a second claimed species of "...providing a ground ring on an inside of the cavity, the ground ring comprising, a first ground ring portion, accessible from the first surface of the substrate, a second ground ring portion, accessible from the second surface of the substrate, and a ground ring trace portion, to electrically connect the first ground ring portion to the second ground ring portion..."

Currently, there is no generic claim, and since applicant has received an action on the merits for the originally presented invention of subject matter of the first claimed species of mounting a die adapter to the semiconductor device, Group II, claims 21,12, and 14 has been constructively elected by original presentation and examination for prosecution on the merits.

Accordingly, Group II, new Claims 21,12,14 are constructively withdrawn from consideration as being directed to a non-elected species. See 37 CFR 1.142(b) and MPEP § 821.03.

2. This application contains claims 21,12,14 drawn to an invention constructively nonelected in this office action. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

3. Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bond et al (5,991,156) in view of Li (5,982,621).

Bond et al teach (at Figs 3-4; col 5, lines 1-49; and Figs 1A-2B; col 3, line 30 through col 4) a method for fabricating an integrated circuit package comprising at least the steps of: providing a substrate having opposite first and second surfaces and conductive traces 22,17 extending there between (Figs 1A-1B; col 3, lines 39-57), the substrate having a cavity therein; fixing a heat sink slug 34 (Fig 3, col 5, lines 1-15) in form of a substantially flat plate to the first surface of the substrate 36/16 (Figs 3,1A) such that the heat slug 34 spans the opening cavity; mounting a semiconductor die 32/12 to said heat slug 34, said semiconductor die 32 being disposed in said cavity; wire bonding 38 said semiconductor die 34 to ones of the conductive traces at the second surface of the substrate (Figs 3-4, col 5, lines 16-23; Fig 1B); encapsulating said wire bonds 38 and said semiconductor die 32 in an encapsulating material 40 (Fig 4; col 5, lines 12-23); and forming a ball grid array on a first surface of said substrate such that bumps 24 of said ball grid array are in electrical connection with ones of said conductive traces 17/22 (Figs 3-4; col 5, lines 24-49; Figs 1A-1B; cols 3-4), wherein the heat slug 34 is fixed to said first surface of said substrate on which the ball grid array is formed; and wherein, as shown in Figures 3-4, the substrate 36 is substantially the same thickness as the semiconductor die 32.

Re claims 15-16, Bond et al lack mounting a die adapter to the semiconductor die; re claim 16; Re claims 17-18, mounting a heat spreader to the substrate; and Re claim 19, mounting a heat spreader such that at least one side wall of the heat spreader is mounted to the substrate and a top portion of the heat spreader contacts the adapter.

However, Re claim 15, Li teaches (at Figs 4-6,2; col 2, line 31 through col 3, line 7) mounting a die adapter 20 to a semiconductor die 31 prior to encapsulating of an encapsulating material 40; Re claim 16, wherein encapsulating comprises encapsulating the wire bonds 32 and the semiconductor die 31 and surrounding the die adapter 20 such that a surface of said die adapter 20 is exposed (Figs 4-6; col 2, lines 31 through col 2, line 7); Re claims 17-18, mounting a heat spreader 10 to the substrate 30 (Figs 4,1-2; col 2, lines 12-31; abstract); and Re claim 19, mounting a heat spreader, prior to encapsulating, such that at least one side wall of said heal spreader 10 is mounted to said substrate 30 and a top portion of said heat spreader contacts said die adapter 20.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the integrated circuit package of Bond by, prior to encapsulating, mounting the die adapter to the semiconductor die and the heat spreader to the substrate such that at least one side wall of said heal spreader is mounted to the substrate and a top portion of the heat spreader contacts the die adapter, as taught by Li. This is because of the desirability to quickly cool the die during operation by dissipating the heat from the chip through the die adapter and the heat spreader, thereby improving the reliability and working efficiency of the integrated circuit package.

4. Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins, III (5,583,377), Suzuki (6,028,358), and Wagner (5,309,322), and further of Li (5,982,621).

Higgins teaches (at Figs 1-8; cols 2-8) a method for fabricating an integrated circuit package comprising at least the steps of: providing a substrate having opposite first and second surfaces and conductive traces 18,14 extending there between, the substrate having a cavity therein; fixing a heat sink slug in form of a plate (e.g. 66/68 in Fig 3) to the first surface of the substrate 62 such that the heat slug spans 66/68 the opening cavity 20 (e.g. Figs 3, col 5, lines 44 through col 6; col 2, line 50 through col 3, line 42), wherein the base portion of heat sink slug preferably extends below circuitized substrate; however, the base portion can be planar with the circuitized substrate (col 6, lines 60-68; lines 7-68; col 8, lines 49-51); mounting a semiconductor die 13 to said heat slug 66, at least a portion of said semiconductor die 13 being disposed in said cavity 20; wire bonding 19 said semiconductor die 13 to ones of the conductive traces 14/18 at the second surface of the substrate 62 (Figs 3,2,1, col 3, line 11 through col 5); encapsulating said wire bonds 19 and said semiconductor die 13 in an encapsulating material 33 (col 4, lines 35-42), and forming a ball grid array 21 on a first surface of said substrate 62 such that bumps 21 of said ball grid array are in electrical connection with ones of said conductive traces 14 (col 3, lines 30-42), wherein fixing the heat slug is fixed to said substrate comprises fixing said heat slug 66/68 to said first surface of said substrate 62 (Fig 3; col 5, lines 44-67; col 2, lines 50 through col 3, line 42; col 4); and wherein, as shown in Figure 3, the substrate 62 is about the same thickness as the semiconductor die 13, with the semiconductor die 13 to be planar with the surface of the substrate 62 (Figure 3; and col 8, lines 14-20 and 50-56; and col 6, lines 41-67).

Higgins already teaches spanning the opening cavity 20 with a heating slug in the form of a plate having the base portion of heat plug preferably extending below circuitized substrate; however, the base portion can be planarized with the circuitized substrate (col 6, lines 60-68; 7-68; and col 8, lines 49-51).

Re claim 15, Higgins lacks showing the heat slug in the form of a substantially flat plate, wherein substrate is substantially the same thickness as the semiconductor die.

However, Suzuki teaches and shows at Figure 1A (first embodiment, col 3, line 55 through col 4) spanning the opening cavity with a heating slug 4 in the form of a plate having the base portion of heat sink plug extending below circuitized substrate, and also teaches and show at Figure 3 (second embodiment; col 5, lines 39-55; Figs 7-8; col 6, line 45 through col 7; Fig 9, col 7, lines 15-24) spanning the opening cavity with a heating slug 13 in the form of a substantially flat plate. In Higgins, as shown in Figure 3, the substrate 62 is about the same thickness as the semiconductor die 13, with the semiconductor die 13 to be planar with the surface of the substrate 62 (Figure 3; and col 8, lines 14-20 and 50-56; and col 6, lines 41-67). Wagner further teaches providing the substrate 24 is substantially the same thickness as the semiconductor die 26 (col 3, lines 55-63; Fig 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fixing the heat slug in the form of the plate of Higgins to the substrate by alternatively employing the heat slug in the form of a substantially flat plate as shown and prima facie taught by Suzuki, wherein Suzuki prima facie teaches forming a heating slug 13 in the form of a substantially flat plate (see Figure 3) instead of using the heat slug 4 having sidewalls and flanges as shown in Figure 1A of Suzuki. This is because these heat slugs are alternative and art recognized equivalent for substitution, wherein a semiconductor device package having the flat heat slug is planar, and wherein a plurality of semiconductor device packages having the flat heat slugs can be effectively stacked together so as to form stacked devices. Additionally, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the semiconductor device of Higgins by making the substrate to have substantially the same thickness of the semiconductor die, as further taught by Wagner. This is because of the desirability to minimize the length of bonding wires, and because of the desirability to form the semiconductor integrated circuit package having a substantially planar surface and structure.

Re further claim 15, Higgins also lacks mounting a die adapter to the semiconductor die (as recited in claims 15-16), mounting a heat spreader to the substrate (as recited in claims 17-18), and mounting a heat spreader such that at least one side wall of the heat spreader is mounted to the substrate and a top portion of the heat spreader contacts the adapter (as recited in claim 19).

However, prior to encapsulating of an encapsulating material 40, Li teaches (at Figs 4-6,2; col 2, line 31 through col 3, line 7), Re claim 15, mounting a die adapter 20 to a semiconductor die 31; Re claim 16, wherein encapsulating comprises encapsulating the wire bonds 32 and the semiconductor die 31 and surrounding the die adapter 20 such that a surface of said die adapter 20 is exposed (Figs 4-6; col 2, lines 31 through col 2, line 7); Re claims 17-18, mounting a heat spreader 10 to the substrate 30 (Figs 4,1-2; col 2, lines 12-31; abstract); and Re claim 19, mounting a heat spreader, prior to encapsulating, such that at least one side wall of said heal spreader 10 is mounted to said substrate 30 and a top portion of said heat spreader contacts said die adapter 20.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fabricate the integrated circuit package of the references including Higgins by, prior to encapsulating, mounting the die adapter to the semiconductor die and the heat spreader to the substrate such that at least one side wall of said heal spreader is mounted to the substrate and a top portion of the heat spreader contacts the die adapter, as taught by Li. This is because of the desirability to quickly cool the die during operation by dissipating the heat from the chip through the die adapter and the heat spreader, thereby improving the reliability and working efficiency of the integrated circuit package.

Response to Amendment

5. Applicant's arguments filed March 19, 2007 with respect to pending claims 15-19 have been considered but they are not persuasive.

Applicant remarked (at 3/19/07 remark page 7) that "...Li discloses mounting a 'tapered heat conductive block 20...made of metal'...This heat conductive block is merely a heat sink, and is not a die adapter as would be understood by one of ordinary skill in the art at the time of the invention. A solid block of metal is not suitable for use as a die adapter...".

In response, this is noted and found unconvincing. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978). Herein, Li clearly teaches using the heat conductive block 20 as a die adapter as claimed, would have been obvious to one of ordinary skill in the art, and would be understood by one of ordinary skill in the art at the time the invention was made.

The Examiner recognizes that references cannot be arbitrarily combined and that there must be some logical reason why skilled in the art would be motivated to make the proposed combination of references. In re Regel 188 USPQ 136 (CCPA 1975). The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin 170 USPQ 209 (CCPA 1971): In Re Rosselet 146 USPQ 183 (CCPA 196). References are evaluated by what they collectively suggest to one versed in the art, rather than by their specific disclosures. In Re Simon, 174 USPQ 114 (CCPA 1972); In Re Richman 165 USPQ 509, 514 (CCPA 1970).

In response to applicant's apparent argument that the applicant has different reason for, or advantage resulting from doing what the prior art relied upon has suggested, it is noted that it is well settled that this is not demonstrative of non-obviousness, In Re Kronig 190 USPQ 425, 428 (CCPA 1976); In Re Lintner 173 USPQ 560 (CCPA 1972); the prior art motivation or advantage may be different than that of applicant while still supporting a conclusion of obviousness. In Re Wiseman 201 USPQ 658 (CCPA 1979); Ex Parte Obiaya 227 USPQ 58 (Bd. of App. 1985).

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Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-3-9

Michael Trinh
Primary Examiner